1. In a system that includes a system memory, and a plurality of processors and one or more other memory consumers that each access the system memory through a memory controller, a method for the memory controller to manage access to the system memory for each of the plurality of processors and the one or more other memory consumers, the method comprising the following:

an act of the memory controller allotting a first division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a first processor of the plurality of processors such that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles; and

an act of the memory controller allotting a second division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a second processor of the plurality of processors such that memory access is conditionally granted to the second processor during the second division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

2. A method in accordance with Claim 1, wherein the first division in a given memory access cycle of the plurality of memory access cycles is before the second division in the given memory access cycle.

3. A method in accordance with Claim 1, wherein the first division in a given memory access cycle of the plurality of memory access cycles is after the second division in the given memory access cycle.

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4. A method in accordance with Claim 1, wherein the first division in a given memory access cycle of the plurality of memory access cycles is adjacent in time with the second division in the given memory access cycle.

5. A method in accordance with Claim 1, wherein the first division in a given memory access cycle of the plurality of memory access cycles is separated in time with the second division in the given memory access cycle by one or more other divisions.

6. A method in accordance with Claim 1, further comprising the following:

an act of receiving a request to access the system memory from the second processor during the second division of the first memory access cycle of the plurality of memory access cycles;

an act of determining that at least one of the one or more other memory consumers has not also requested access to the system memory during the second division of the first memory access cycle; and

in response to the act of determining that at least one of the one or more other memory consumers has not also requested to access the system memory and the act of receiving the request from the second processor, an act of imposing the request from the second processor on the system memory.

7. A method in accordance with Claim 6, wherein the act determining that at least one of the one or more other memory consumers has not also requested access to the system memory during the second division of the first memory access cycle comprises the following:

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an act of concluding that the at least one of the one or more other memory consumers has not also requested access based on having received the request to access system memory from the second processor, wherein the request is not issued by the second processor if the at least one of the one or more memory consumers had requested access.

8. A method in accordance with Claim 6, wherein the act determining that at least one of the one or more other memory consumers has not also requested access to the system memory during the second division of the first memory access cycle comprises the following:

an act of concluding that the at least one of the one or more other memory consumers has not also requested access based on having received the request to access system memory from the second processor, wherein the request from the second processor is not received by the memory controller if the at least one of the one or more memory consumers had requested access.

9. A method in accordance with Claim 6, further comprising the following:

an act of determining that the at least one of the one or more other memory consumers has requested access to the system memory during the second division of a second memory access cycle of the plurality of memory access cycles; and

an act of allowing the at least one of the one or more other memory consumers to have access to the system memory during the second division of the second memory access cycle.

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10. A method in accordance with Claim 9, wherein the first memory access cycle is before the second memory access cycle.

11. A method in accordance with Claim 9, wherein the first memory access cycle is after the second memory access cycle.

12. A method in accordance with Claim 9, wherein the second memory access cycle is adjacent in time with the first memory access cycle.

13. A method in accordance with Claim 9, wherein the second memory access cycle is separated in time with the first memory access cycle by one or more other memory access cycles.

14. A method in accordance with Claim 9, further comprising the following:

an act of receiving a request from the second processor to access the system memory during the second division of the second memory access cycle, wherein the act of allowing the at least one of the one or more other memory consumers to have access to the system memory during the second division of the second memory access cycles is performed regardless of having received the request from the second processor to access the system memory during the second division of the second memory access cycle.

15. A method in accordance with Claim 1, further comprising the following:

an act of the memory controller allotting a third division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a third

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processor of the plurality of processors such that memory access is guaranteed for the third processor during the third division of each of the plurality of memory access cycles.

16. A method in accordance with Claim 15, further comprising the following:

an act of the memory controller allotting a fourth division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a fourth processor of the plurality of processors such that memory access is conditionally granted to the fourth processor during the fourth division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

17. A method in accordance with Claim 1, further comprising the following:

an act of the memory controller allotting a fourth division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a fourth processor of the plurality of processors such that memory access is conditionally granted to the fourth processor during the fourth division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

18. A method in accordance with Claim 1, wherein at least one of the one or more other memory consumers includes a serial interface.

19. A method in accordance with Claim 1, wherein the one or more memory consumers comprise a plurality of memory consumers.

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20. A system comprising the following:

a system memory,

a memory controller that governs access to the system memory;

a plurality of processors that each access the system memory through the memory controller; and

one or more other memory consumers that also each access the system memory through the memory controller, wherein

the memory controller is configured to perform the following:

an act of allotting a first division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a first processor of the plurality of processors such that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles; and

an act of allotting a second division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a second processor of the plurality of processors such that memory access is conditionally granted to the second processor during the second division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

21. A system in accordance with Claim 20, wherein the memory controller is further configured to perform the following:

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an act of receiving a request to access the system memory from the second processor during the second division of the first memory access cycle of the plurality of memory access cycles;

an act of determining that at least one of the one or more other memory consumers has not also requested access to the system memory during the second division of the first memory access cycle; and

in response to the act of determining that at least one of the one or more other memory consumers has not also requested to access the system memory and the act of receiving the request from the second processor, an act of imposing the request from the second processor on the system memory.

22. A system in accordance with Claim 21, wherein the memory controller is further configured to perform the following:

an act of determining that the at least one of the one or more other memory consumers has requested access to the system memory during the second division of a second memory access cycle of the plurality of memory access cycles; and

an act of allowing the at least one of the one or more other memory consumers to have access to the system memory during the second division of the second memory access cycle.

23. A system in accordance with Claim 20, wherein the memory controller is further configured to perform the following:

an act of allotting a third division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a third processor of the plurality of

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processors such that memory access is guaranteed for the third processor during the third division of each of the plurality of memory access cycles.

24. A system in accordance with Claim 23, wherein the memory controller is further configured to perform the following:

an act of allotting a fourth division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a fourth processor of the plurality of processors such that memory access is conditionally granted to the fourth processor during the fourth division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

25. A system in accordance with Claim 20, wherein the memory controller is further configured to perform the following:

an act of allotting a third division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a third processor of the plurality of processors such that memory access is conditionally granted to the third processor during the third division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

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26. A system in accordance with Claim 20, wherein at least one of the one or more other memory consumers includes a serial interface.

27. A system in accordance with Claim 20, wherein the one or more memory consumers comprise a plurality of memory consumers.

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28. A memory controller configured to perform the following when operated in a system that includes a system memory for which the memory controller governs access, and a plurality of processors and one or more other memory consumers that each access the system memory through the memory controller:

an act of allotting a first division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a first processor of the plurality of processors such that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles; and

an act of allotting a second division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a second processor of the plurality of processors such that memory access is conditionally granted to the second processor during the second division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

29. A memory controller in accordance with Claim 28, further configured to perform the following:

an act of receiving a request to access the system memory from the second processor during the second division of the first memory access cycle of the plurality of memory access cycles;

an act of determining that at least one of the one or more other memory consumers has not also requested access to the system memory during the second division of the first memory access cycle; and

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in response to the act of determining that at least one of the one or more other memory consumers has not also requested to access the system memory and the act of receiving the request from the second processor, an act of imposing the request from the second processor on the system memory.

30. A memory controller in accordance with Claim 29, further configured to perform the following:

an act of determining that the at least one of the one or more other memory consumers has requested access to the system memory during the second division of a second memory access cycle of the plurality of memory access cycles; and

an act of allowing the at least one of the one or more other memory consumers to have access to the system memory during the second division of the second memory access cycle.

31. A memory controller in accordance with Claim 28, further configured to perform the following:

an act of allotting a third division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a third processor of the plurality of processors such that memory access is guaranteed for the third processor during the third division of each of the plurality of memory access cycles.

32. A memory controller in accordance with Claim 31, further configured to perform the following:

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an act of allotting a fourth division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a fourth processor of the plurality of processors such that memory access is conditionally granted to the fourth processor during the fourth division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

33. A memory controller in accordance with Claim 28, further configured to perform the following:

an act of allotting a third division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a third processor of the plurality of processors such that memory access is conditionally granted to the third processor during the third division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

34. A memory controller in accordance with Claim 28, wherein the memory controller is implemented in a laser transmitter/receiver.

35. A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is a 1G laser transceiver.

36. A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is a 2G laser transceiver.

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37. A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is a 4G laser transceiver.

38. A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is a 10G laser transceiver.

39. A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is a laser transceiver suitable for fiber channels greater than 10G.

40. A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is an XFP laser transceiver.

41. A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is an SFP laser transceiver.

42. A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is a SFF laser transceiver.

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